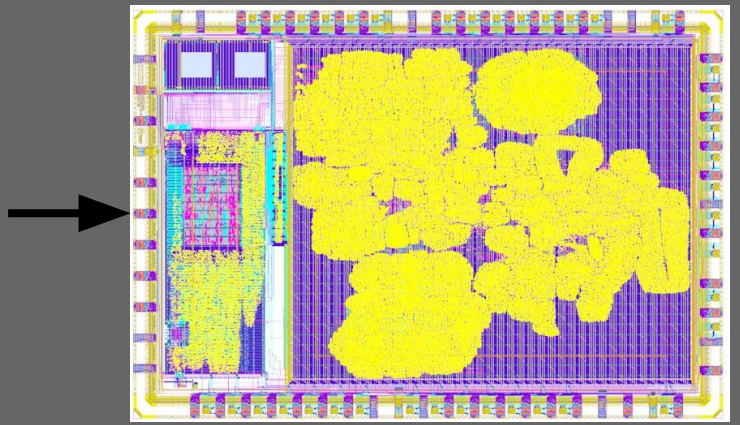
CPE 470 - Openlane Continued

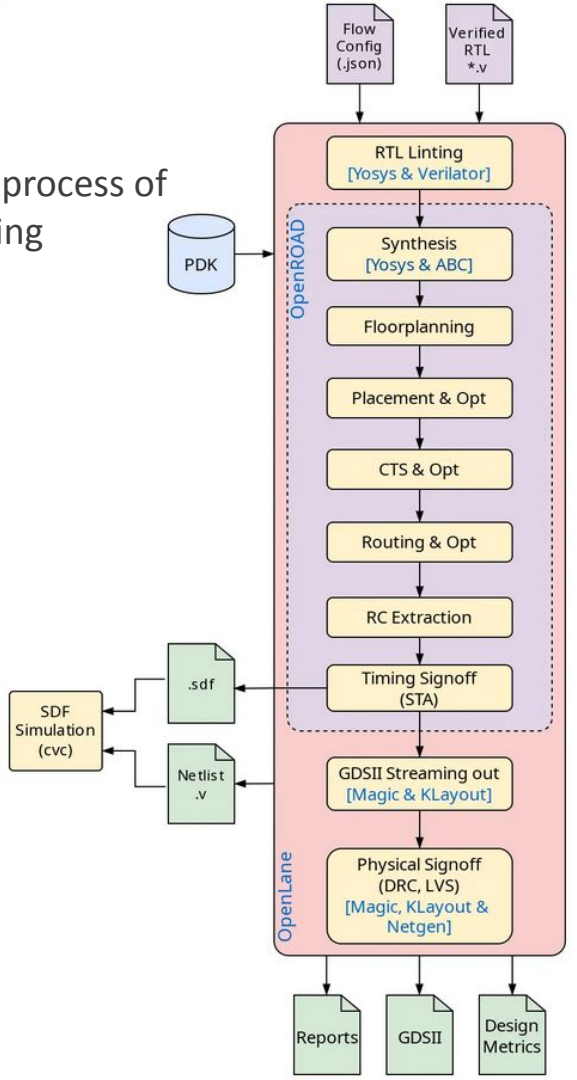


EDA Design Flows

- Last time we got through
  - Linting
  - Synthesis
  - Post Synthesis STA
- Today we will finish
  - **PNR**
    - CTS
  - Post PNR STA
  - DRC
  - LVS

Glossary

PNR: Place and Route, process of arranging and connecting components



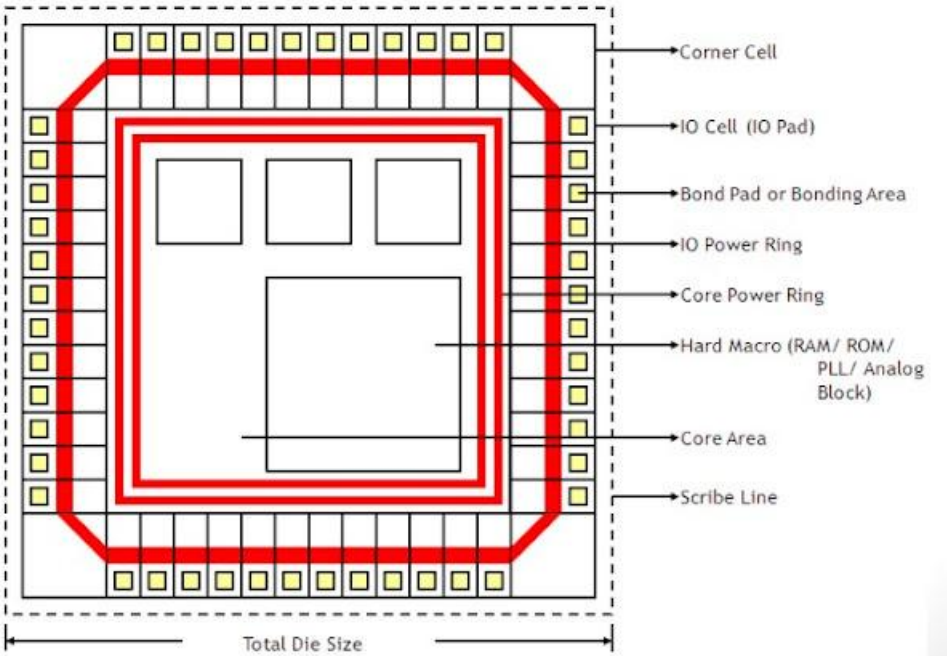
Floorplanning

- Floorplanning decides generally how big chip is and where things go
  - **Macros** placed manually
  - Standard cell locations estimated
- **Core Utilization** (`FP_CORE_UTIL`)
  - Averages 50-60%
  - **Higher** utilization → greater logic density, more gates
    - Might fail in routing
  - **Lower** utilization → less gates, but easier to route
- Floorplan sizing types (`FP_SIZING`)
  - **Absolute**: chip has set dimensions
    - Die area will be set to:
    - "x0 y0 x1 y1"
  - **Relative**: chip will scale to size of logic

Glossary

Macros: pre-laid-out circuits to use as a component in a design. Often memory, IP, or analog circuitry

Core Utilization: percentage of area used for logic versus kept empty for routing

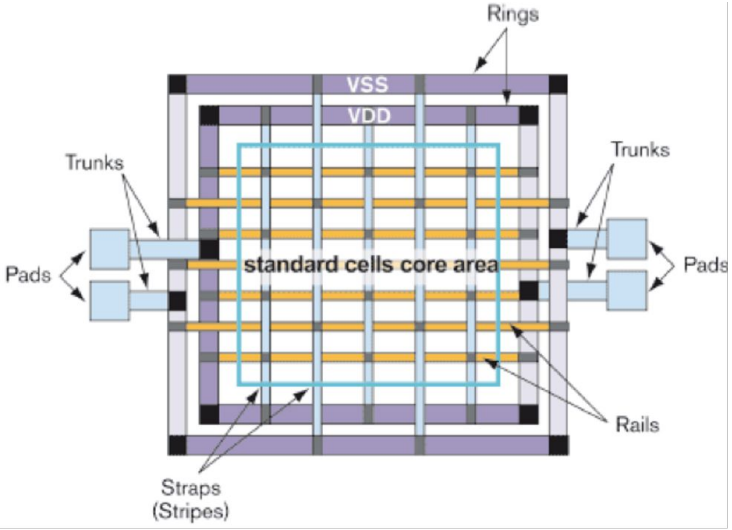


Power Connections

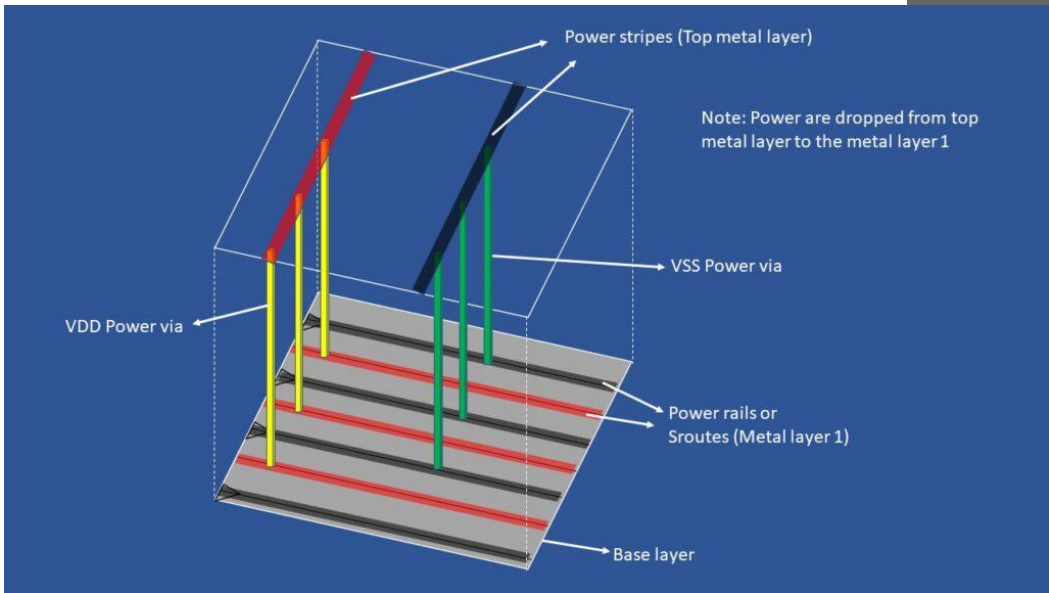
Glossary

PDN: Power Distribution Network

- Every standard cell needs power
  - **PDN** used to globally route power
- Standard Cells exist in rows between Power and Ground rails
- Localized Power Rails are fed by global straps (stripes)

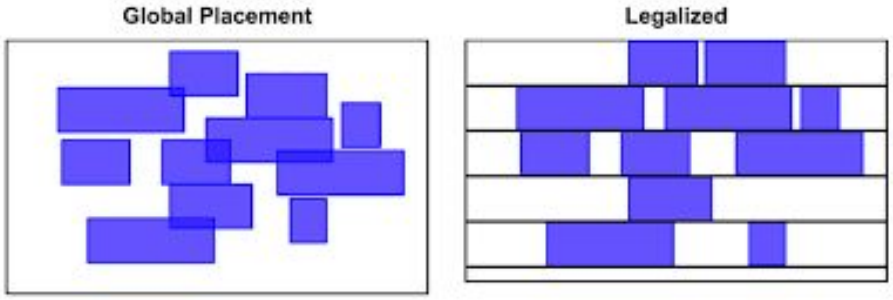


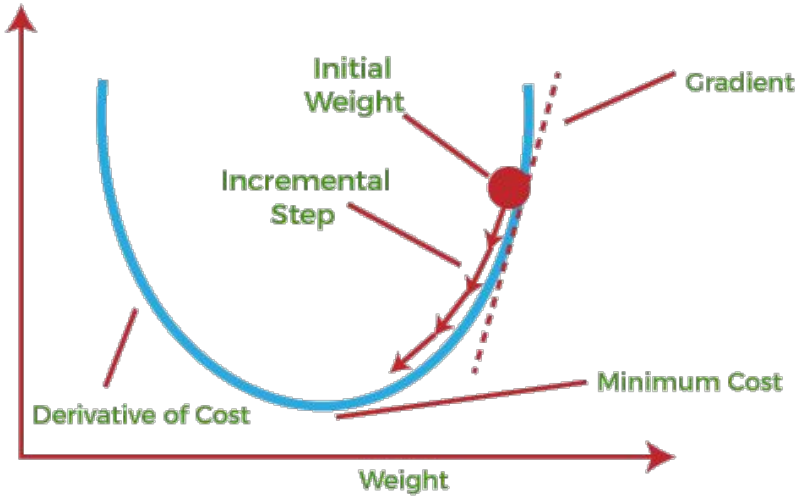
This figure show the complete power planning.



Placement

- Tools must place every standard cell, intelligently
  - Start with **semi-random** placement
  - Use **wire length** and/or delay as a **cost function**
    - Involved logic gates should end up close together
  - **Optimize** by **swapping** or moving gates
    - Similar to gradient descent in AI: find local minimums
  - Can change number of iterations to further (or over) optimize
- **Legalization**: move standard cells from general positions into strict rows



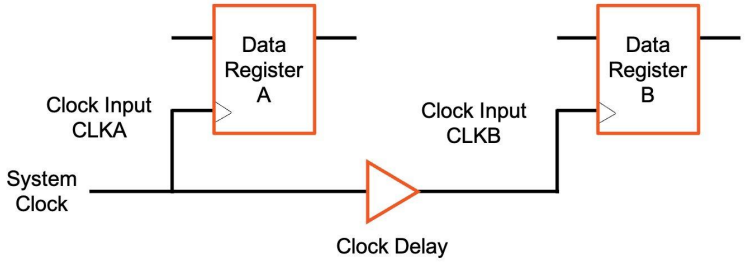


Clock Tree Synthesis - Skew

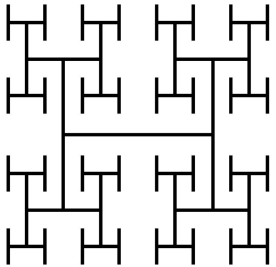
Glossary

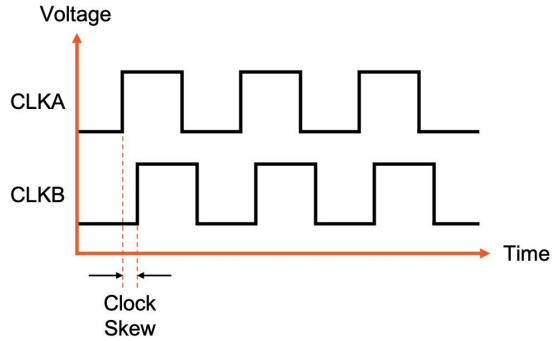
CTS: Clock Tree Synthesis
Clock Skew: difference in clock signal arrival time between points

- Important that clock signals globally arrive at the same time
  - Difference in arrival times is clock skew
- **Clock Skew** makes all timing violations worse
  - Clock arrives early ⟶ risk Setup Violation
  - Clock arrives late ⟶ risk Hold Violation
- Use specialized structures to distribute clock signal
  - H Trees -> fractals
  - Same propagation delay to every endpoint



H Tree



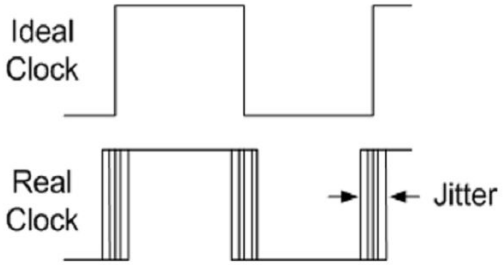


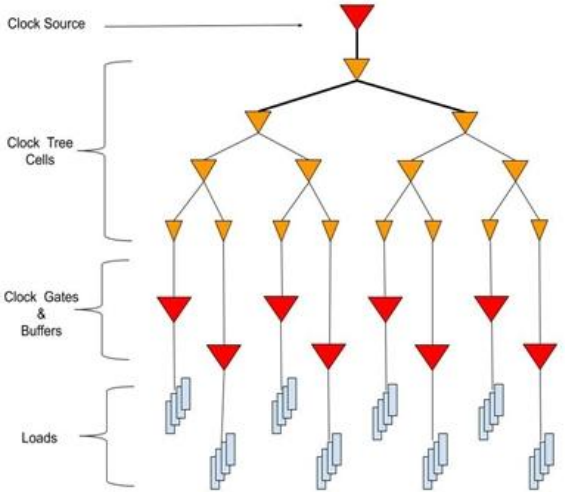
Clock Tree Synthesis - Jitter

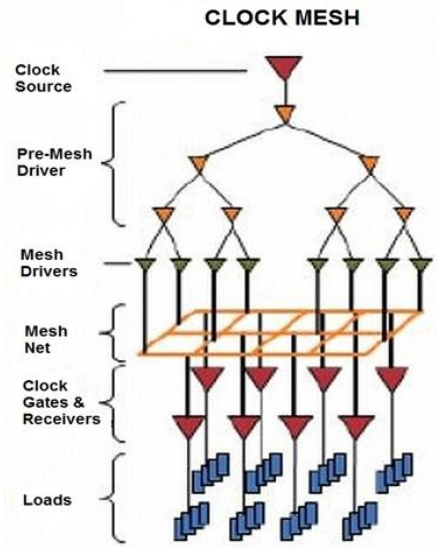
- Clock Cells ⟶ specialized standard cells that maximize consistency
  - Try not to introduce **Clock Jitter**
- Clock Tree
  - Create H tree that reaches every single clocked endpoint
- Clock Mesh
  - Global scale clock tree drives local scale meshes
  - Slightly worse skew but easier routing

Glossary

Clock Jitter: inconsistencies in the edge placement of a clock over time





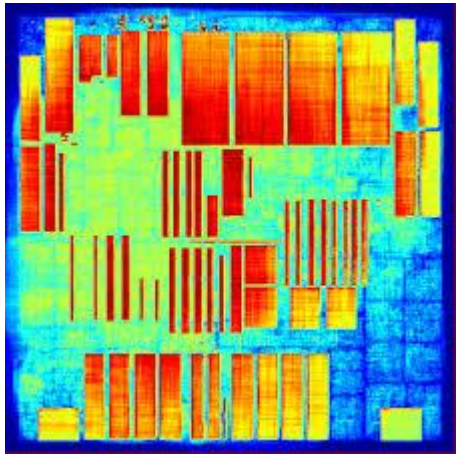


Routing

Glossary

Congestion: ratio of how much available routing space is being used

- Modern chips are wire limited, not logic limited
  - Can fit all the gates we want
  - Wiring them up becomes much harder
- Routing: uses metal layers and vias to connect gates as needed
- Directionality:
  - Generally each layer has a preferred direction
  - IE. metal2 is horizontal, metal3 is vertical
- Run into **congestion** issues in dense areas
  - 100% congestion → no more wires in an area
  - Turn down core utilization
  - Refactor global signals



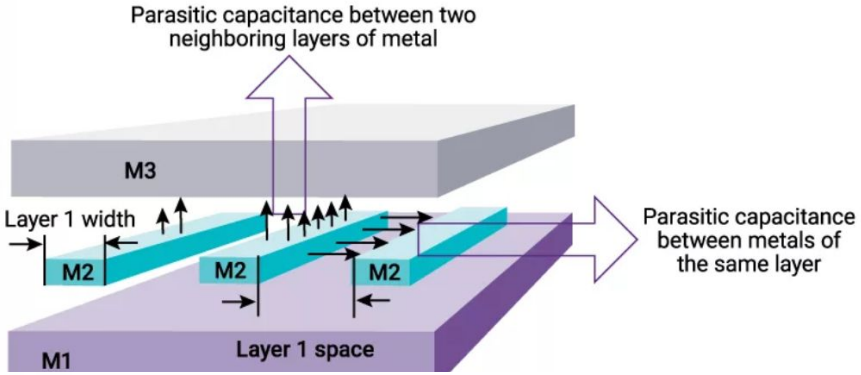
Congestion Heatmap: Visualizes areas with many interconnects, where wire space is all used up

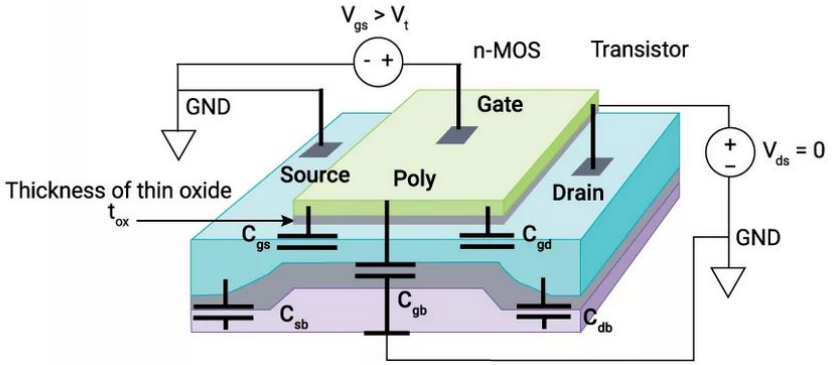
RC Extraction for STA

Glossary

PEX: Parasitic Extraction
Parasitics: unintended resistance, capacitance, etc. inherent to physical design

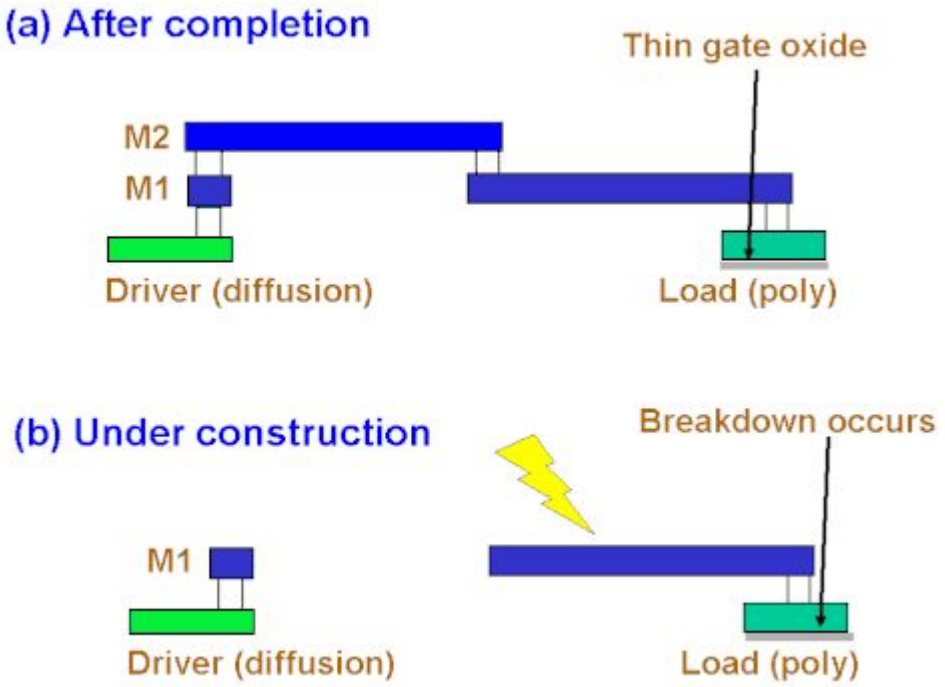
- Extract Resistance and Capacitance values of each cell and wire using **PEX**
  - Analyze wire and gate area, length
  - Calculate **parasitics**
- Use extracted values to more accurately model delay
- Re-run **STA** using higher-accuracy model
  - Previously, modeled cells and wires with less accurate delay estimates
  - Now takes account for all gate sizes and wire lengths
- Well Laid-Out Chip
  - Timing might improve
- Long Global Wires
  - Timing worse than estimated





Antennae Checking

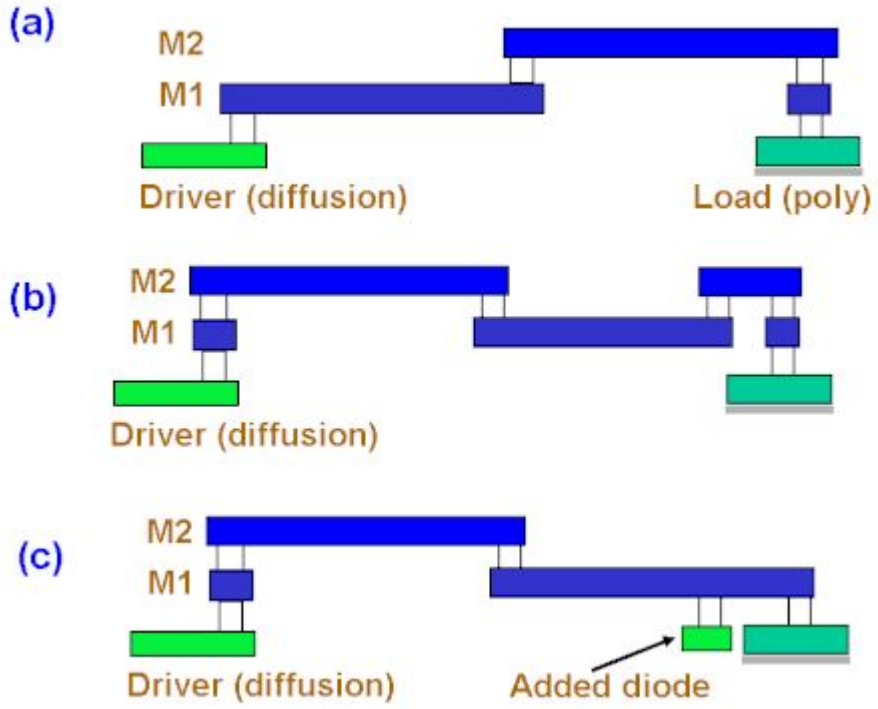
- Not Noise Related!
- Risk of damage during manufacturing of long wires
  - **“plasma induced gate oxide damage”**
- Metal layers are etched with plasma ⟶ Large Static Charges
- Transistor gates are sensitive to high voltage
  - Will spark and destroy gate
- Means long wires can physically break your design



Antennae Solutions

To fix this, tell the tools to keep trying with `GRT_ANTENNA_ITERS`

a. Change routing layers
   - Try not using lowest metal layer near gates
b. Add vias near gates
   - Prevent charge buildup
c. Diode Insertion
   - Insert protective diodes near sensitive gates to provide alternate static discharge path

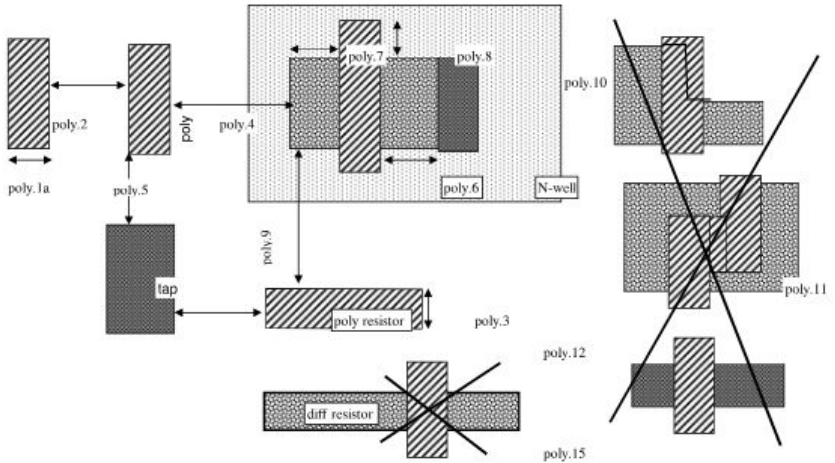


Glossary

DRC: Design Rule Checking

DRC

- Ensures manufacturability
- Enforces rules set by the PDK about what is allowed for each layer
- Most computationally intensive
  - Needs to calculate geometry of thousands to millions of shapes across hundreds of layers
  - Can take hours
- Can skip while in early stages of design
  - `openlane --skip magic.drc --skip klayout.drc ...`
  - Do not skip for a final design!!



SPICE Extraction

Glossary

SPICE: Simulation Program with Integrated Circuit Emphasis, electrical simulation language used in LTSpice, NGSpice, etc.

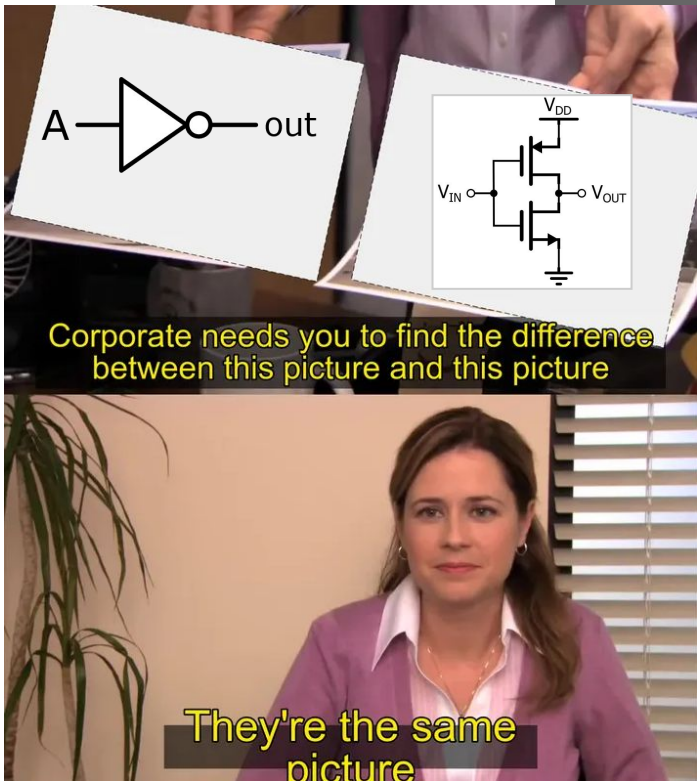
- Use geometry of wires and gates to assemble an electrical netlist (a **SPICE** model)
  - Metal layers connected by vias become single nets
- Assemble transistor-level or gate-level electrical model of system
  - Can do electrical simulation of small scale systems
  - Extremely computationally intensive and slow, much worse than logic simulation

Glossary

LVS: Layout Versus Schematic

Layout Versus Schematic

- **LVS** compares the electrical **SPICE** netlist of the final circuit with the expected synthesized logical netlist
- Should match if the tools did their job
  - Doesn't match? LVS Error
- Common Issues with LVS:
  - Power / Ground rails not properly connected
  - `inout` used at the top level
    - Top level should generally not be bidirectional



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